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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/620,474	11/06/2000	Makoto Fujiwara	43889-964	3082

7590 07/16/2003

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/620,474	FUJIWARA, MAKOTO	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-19* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13 and 17-19* is/are rejected.

7)☒ Claim(s) *14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 7-19 of U.S. Application 09/620,474 filed on 07/20/00 are presented for examination. Claims 7-19 were elected for examination by the Applicant in paper #10, in response to the restriction of paper #9. Nonelected claims 1-6 have not been examined.

Election/Restrictions

2. Applicant's election of Claims 7-19 in Paper No. 10 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
3. This application contains Claims 1-6 drawn to an invention nonelected with traverse in Paper No. 10. A complete reply to this Office Action must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Objections

4. Claims 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 7-11 and 18-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, the phrase "applications are limitlessly operated" is indefinite.

7. Claims 11 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, the phrases "generating a ... function part to be disposed in a bus", and "where the number of concurrent instruction processing is larger than a value" are indefinite.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. The prior art used for these rejections is as follows:

10. Mahmud, S.M. "Communication Performance in a Hierarchical Bus System". Int'l Symposium on Circuits and Systems, 1989. May 11, 1989. Vol.1, pp.122-125. (Henceforth referred to a "**Mahmud_1**").

11. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

12. Claims 7, 9-13, 17 and 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Mahmud_1.

13. In regards to Claim 7, Mahmud_1 teaches the following limitations:

7 . A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications, comprising a step of:
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

analyzing a number of collisions of bus transaction through operation simulation where said applications are limitlessly operated by said control function part by successively using each of said plural libraries as the operation model of each of said plural applications.
(Mahmud_1, especially: Fig.6-8 and associated text. Examiner finds that a "conflicts" due to a "blocked" bus is equivalent to a "collision". Examiner finds that bandwidth is therefore a function of the number of collisions.)

14. In regards to Claim 9, Mahmud_1 teaches the following limitations:

9 . A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications, comprising a step of:
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

analyzing a number of concurrent instruction processing through operation simulation where said applications are limitlessly operated by said control function part by successively using each of said plural libraries as the operation model of each of said plural applications.
(Mahmud_1, especially: Fig.6-8 and associated text. Examiner finds "concurrent instruction processing" is inherent in a multi-processor, multi-memory system)

15. In regards to Claim 10, Mahmud_1 teaches the following limitations:

10. The method of designing an interface of Claim 9,
wherein a structure of a cross bar bus is determined in accordance with the number of concurrent instruction processing.
(Mahmud_1, especially: Figs.1-3, and p.122, col.1.)

16. In regards to Claim 11, Mahmud_1 teaches the following limitations:

11. The method of designing an interface of Claim 10, further comprising a step of generating a transfer operation control function part to be disposed in a bus where the number of concurrent

instruction processing is larger than a value,
(Mahmud_1, especially: Figs.1-3, and p.122, col.1.)

wherein the number of concurrent instruction processing is analyzed with the transfer operation control function part disposed in the bus.
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text.)

17. In regards to Claim 12, Mahmud_1 teaches the following limitations:

12 . A method of designing an interface for connection between
a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications and plural bus structures, comprising the steps of:
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

(a) setting plural main parameters for ultimately evaluating
said semiconductor integrated circuit and setting plural
sub-parameters affecting each of said main parameters;
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

(b) selecting library groups where said main parameters meet
target values by evaluating each of said main parameters on the
basis of said sub-parameters of each of said libraries; and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

(c) determining an interface by selecting an optimal library
group by evaluating plural main parameters determined with respect
to each of said selected library groups.
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

18. In regards to Claim 13, Mahmud_1 teaches the following limitations:

13 . The method of designing an interface of Claim 12 , further
comprising, before the step (a), a step of analyzing said
sub-parameters of each of said libraries through operation simulation conducted by successively using each of said plural libraries as an operation model of each of said plural applications.
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

19. In regards to Claim 17, Mahmud_1 teaches the following limitations:

17 . A method of designing an interface for connection between a control function part of a semiconductor integrated circuit and plural applications by using a database storing plural libraries corresponding to operation models of said plural applications and
plural bus structures, comprising the steps of:

(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

(a) successively selecting each of said plural libraries as the operation model of each of said plural applications;
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

(b) operating said plural applications by said control function part, whereby analyzing performances of said control function part, an interface and said applications attained by using each of said libraries;
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

(c) repeatedly conducting the steps (a) and (b), whereby determining an interface by selecting an optimal library group on the basis of results of the analysis; and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

(d) synthesizing an optimal interface on the basis of said determined parameters.
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

20. In regards to Claim 19, Mahmud_1 teaches the following limitations:

19. The method of designing an interface of Claim 17,

wherein, in the step (b) , a number of concurrent instruction processing occurring by limitlessly operating said applications by said control function part is analyzed with respect to each of said libraries, and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

in the step (d) , a cross bar bus is disposed in a bus where the number of concurrent instruction processing is larger than a value.
(Mahmud_1, especially: Figs.1-3, and p.122, col.1.)

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The prior art used for these rejections is as follows:

23. Mahmud, S.M. "Communication Performance in a Hierarchical Bus System". Int'l Symposium on Circuits and Systems, 1989. May 11, 1989. Vol.1, pp.122-125. (Henceforth referred to a "**Mahmud_1**").

24. Mahmud, S.M. "Performance Analysis of Multilevel Bus Networks for Hierarchical Multiprocessors". IEEE Transactions on Computers. July 1994. Vol.43, Issue 7, pp.789-805. (Henceforth referred to a "**Mahmud_2**").

25. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

26. Claims 8, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahmud_1 in view of Mahmud_2.

27. In regards to Claim 8, Mahmud_1 does not express the use of FIFOs as claimed in the following limitations:

8 . The method of designing an interface of Claim 7 , further comprising a step of generating FIFOs in a number of stages according to the number of collisions of bus transaction,
(Mahmud_2, especially: Fig.5, and associated text.)

wherein the number of collisions of bus transaction is analyzed with the FIFOs virtually inserted between said applications.
(Mahmud_2, especially: Fig.5, and associated text.)

Mahmud_2, on the other hand, does expressly teach the generation and analysis of buffers ("FIFOs"). (See especially: Fig.5, and associated text – Section IV.B. "Queuing Model of an Asynchronous MLB System").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of

Mahmud_2 because "If read and write references are treated equally ... the entire system behaves like a simple closed-queueing network. But if read and write references are treated differently, the queueing network model becomes a little bit complicated due to the presence of both open and closed class customers. ... It is obvious that more throughput can be obtained from the system if read and write references are treated differently than [if] they are treated equally." (Mahmud_2, p.796, col.1).

28. In regards to Claim 18, Mahmud teaches the following limitations:

18. The method of designing an interface of Claim 17,

wherein, in the step (b), a number of collisions of bus transaction occurring by limitlessly operating said applications by said control function part is analyzed with respect to each of said libraries, and
(Mahmud_1, especially: Fig.3, Fig.6-8, Tables 1 and 2, and associated text. Examiner finds that the tables are a form of a database.)

However, Mahmud_1 does not express the use of FIFOs as claimed in the following limitation:

in the step (d), FIFOs in a number of stages according to the number of collisions of bus transaction are inserted between said applications.
(Mahmud_2, especially: Fig.5 and associated text.)

Mahmud_2, on the other hand, does expressly teach the generation and analysis of buffers ("FIFOs"). (See especially: Fig.5, and associated text – Section IV.B. "Queuing Model of an Asynchronous MLB System").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Mahmud_1 with those of Mahmud_2 because "If read and write references are treated equally ... the entire system behaves like a simple closed-queueing network. But if read and

write references are treated differently, the queueing network model becomes a little bit complicated due to the presence of both open and closed class customers. ... It is obvious that more throughput can be obtained from the system if read and write references are treated differently than [if] they are treated equally." (Mahmud_2, p.796, col.1).

Conclusion

29. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

30. Chang, Y.C. et al. "Design and Performance of a Highly Pipelined Bus for Shared Memory Multiprocessor". Proceedings of the 20th EUROMICRO Conference. Sept. 8, 1994. pp.451-456.

31. Chiung-San, L. et al. "Performance Modelling and Evaluation for the XMP Shared-Bus Multiprocessor Architecture". Int'l Conf. on Parallel and Distributed Systems. Dec. 21, 1994. pp.446-453.

32. Woo-Jong, H. et al. "A Multiprocessor Server with a New Highly Pipelined Bus." Proceedings of the 10th Int'l Parallel Processing Symposium, (IPPS '96). Apr. 19, 1996. pp.512-517.

33. Jiang, H. et al. "PPMB: A Partial-Multiple-Bus Multiprocessor Architecture with Improved Cost-Effectiveness". IEEE Transactions on Computers. Mar. 1992. Vol. 41, Issue 3, pp.361-366.

34. U.S. Patent 5,541,849.

35. U.S. Patent 6,493,351.

36. U.S. Patent 6,516,379.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

Official communications:	(703) 746-7239
Non-Official / Draft communications	(703) 746-7240
After Final communications	(703) 746-7238

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

July 11, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER